

Fig. 1(c)

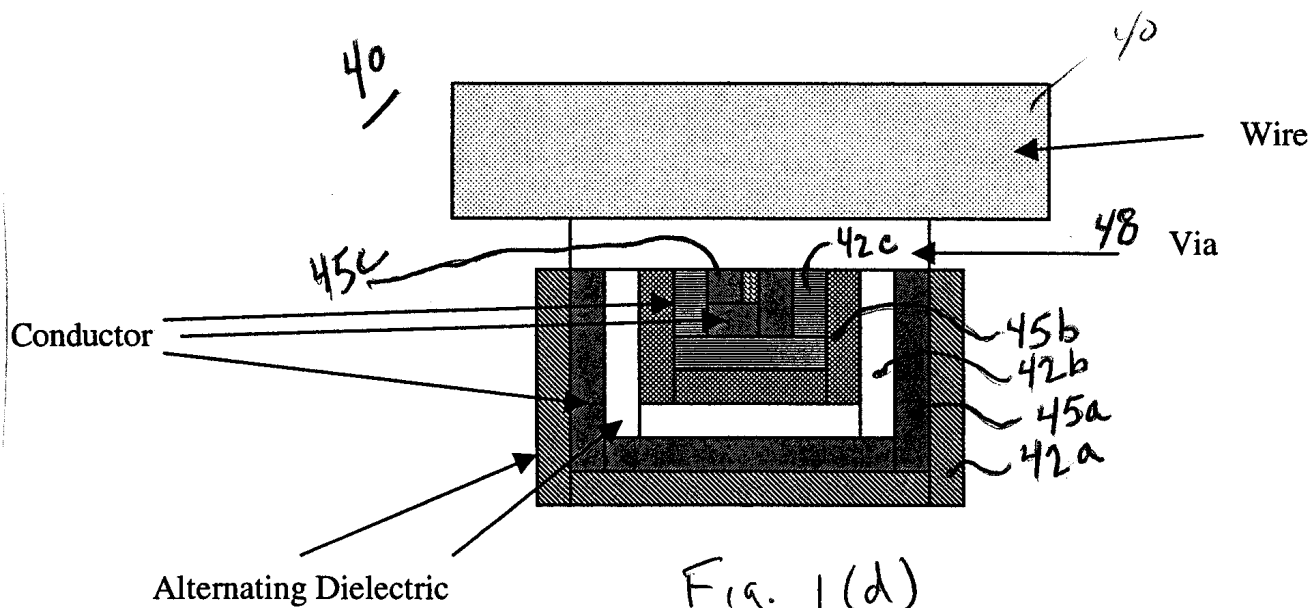


Fig. 1(d)

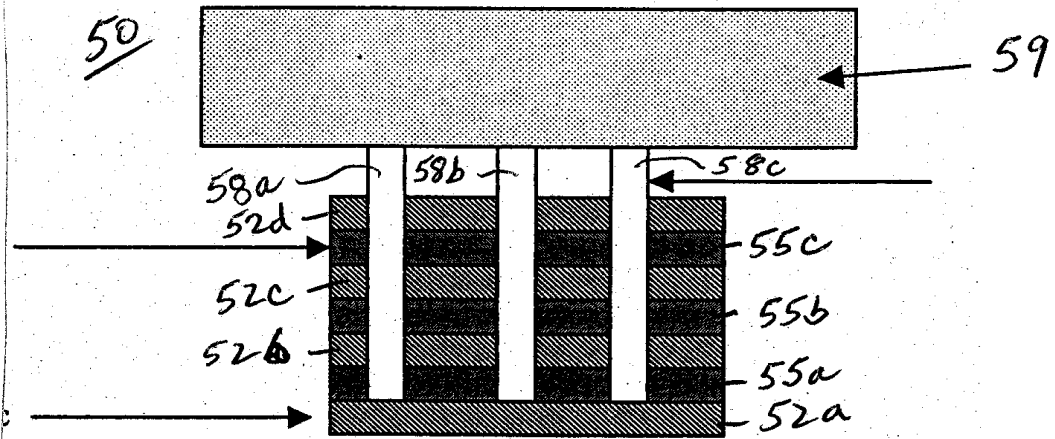


FIG. 2(a)

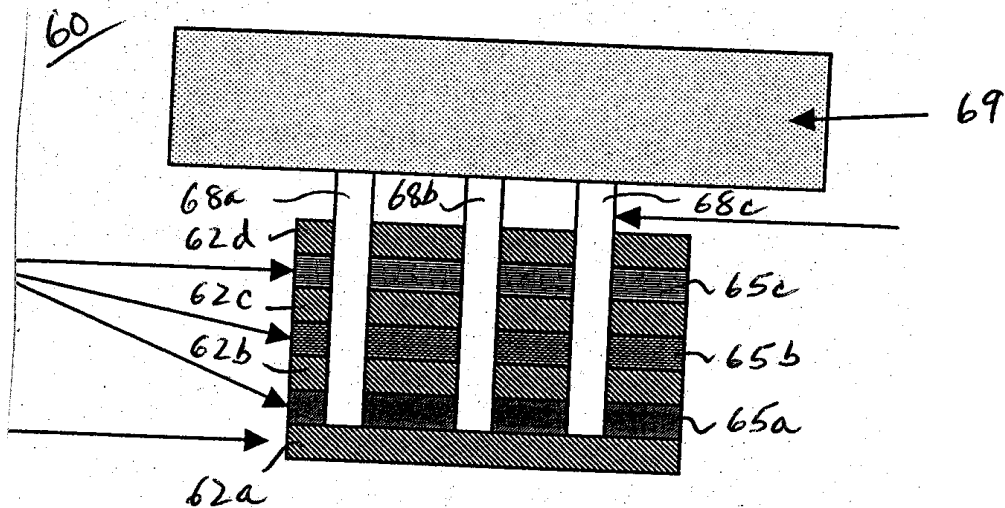


FIG. 2(b)

100

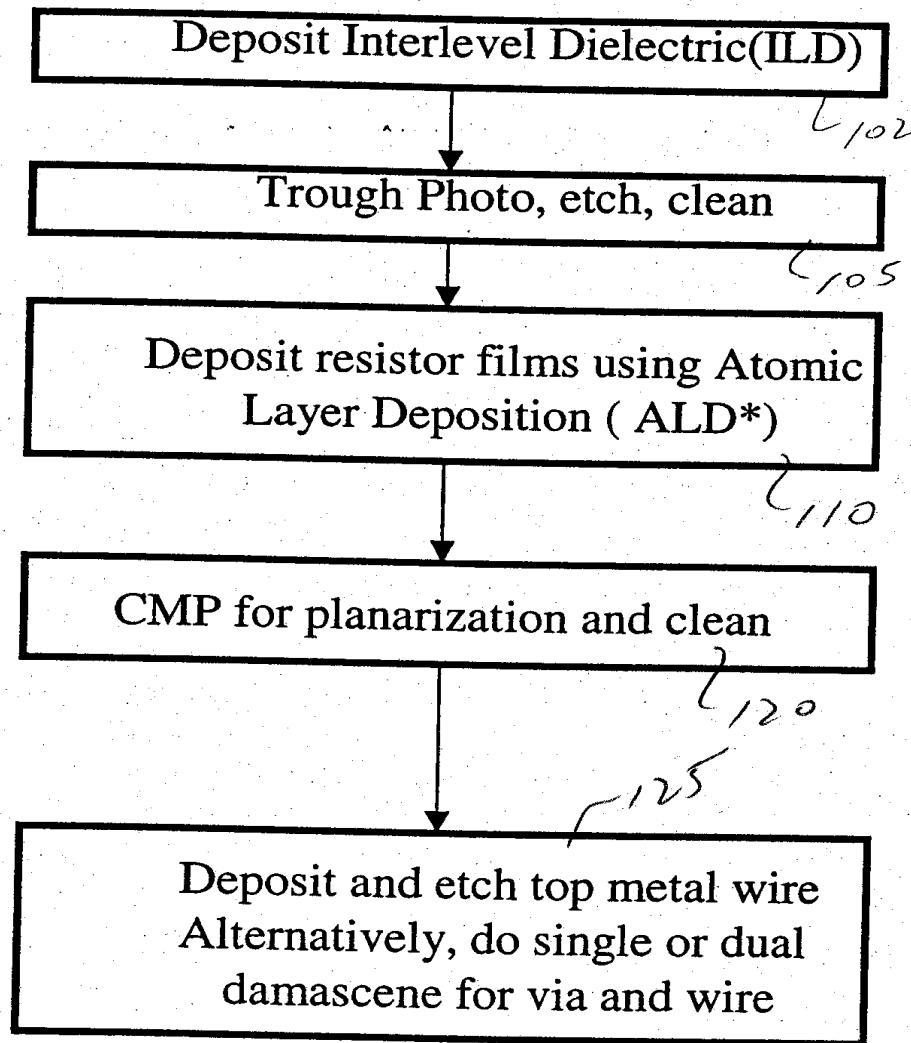


FIG. 3

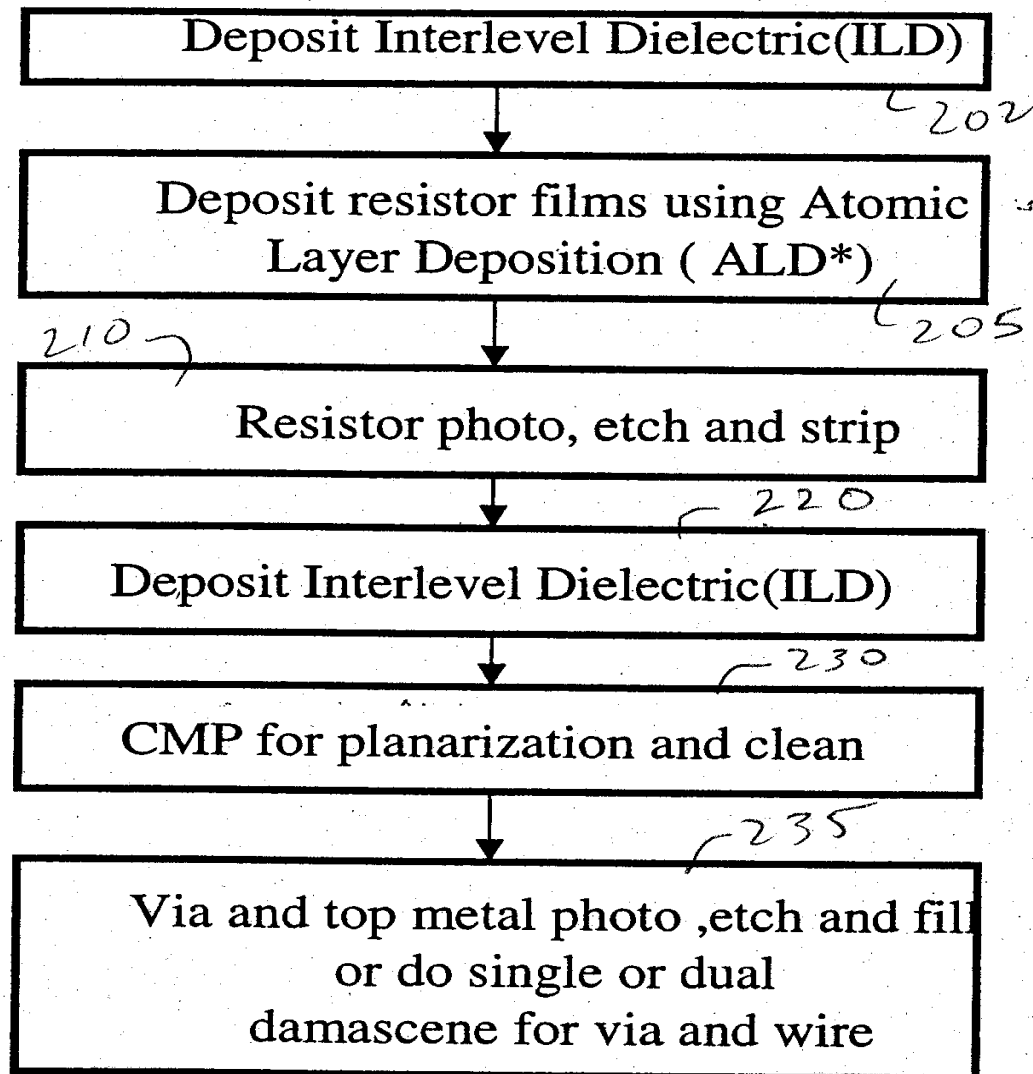


FIG. 4

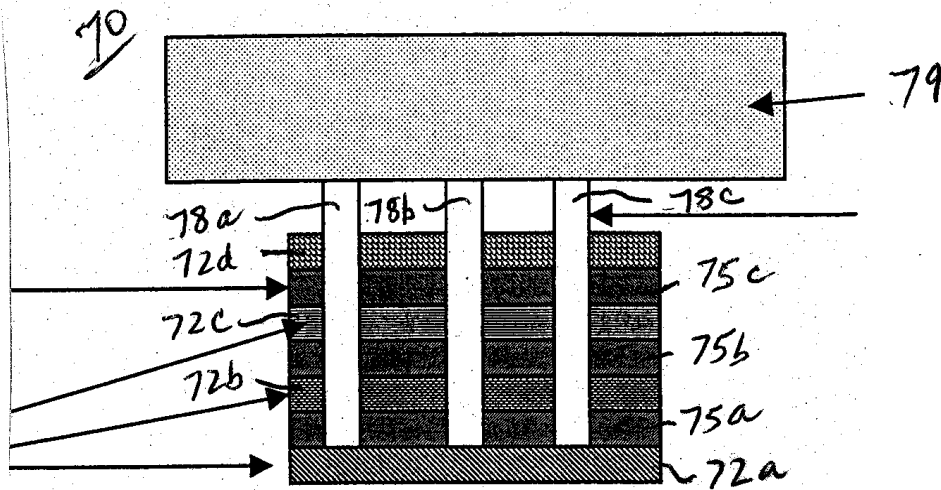


FIG. 2(c)

## Design System

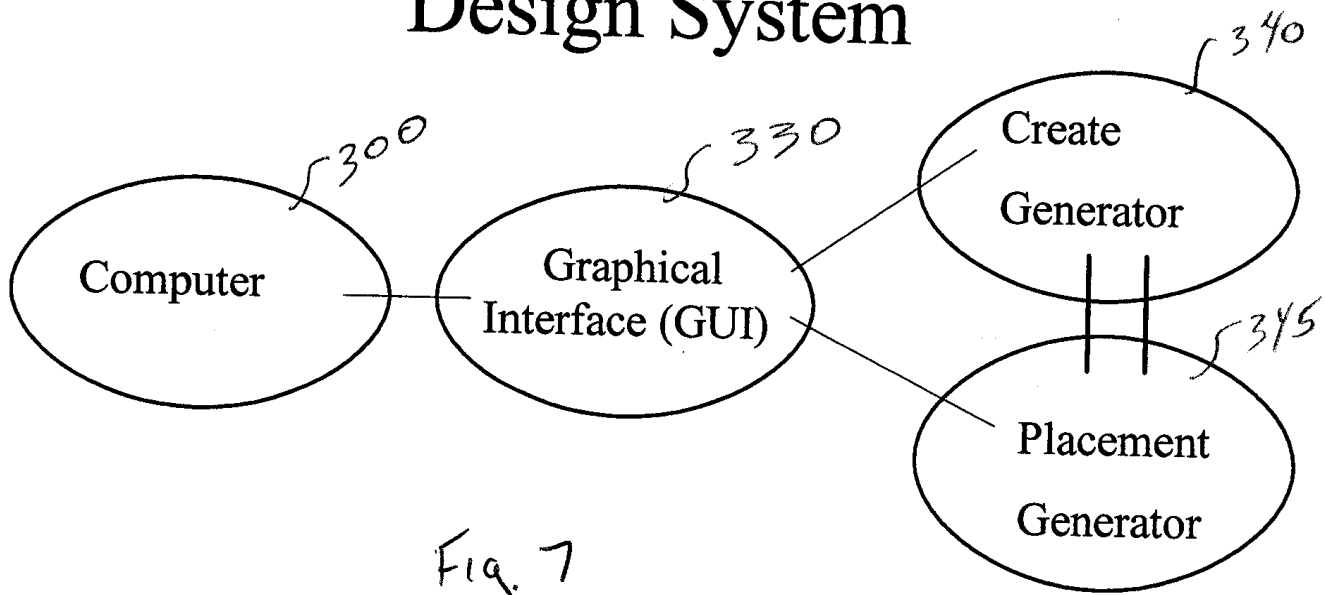


Fig. 7

## Design System

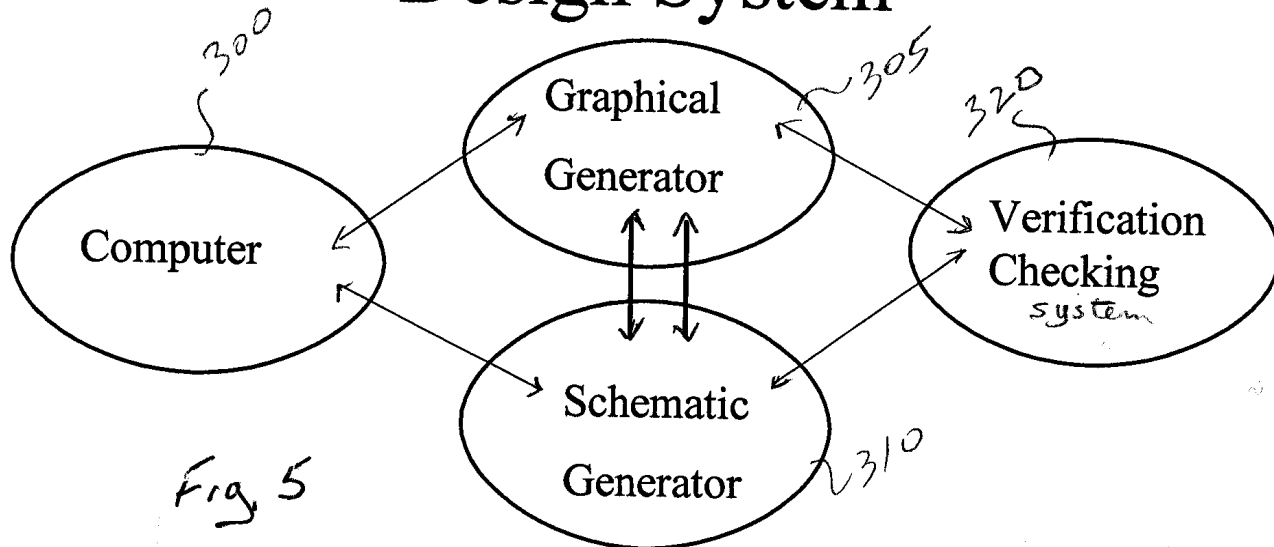


Fig. 5

## Design System

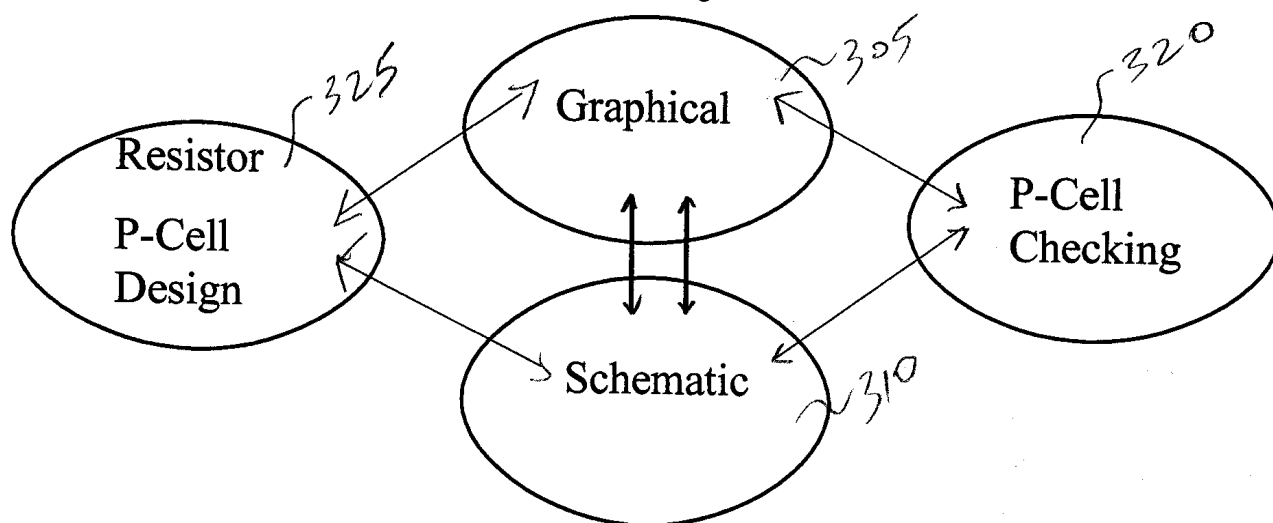
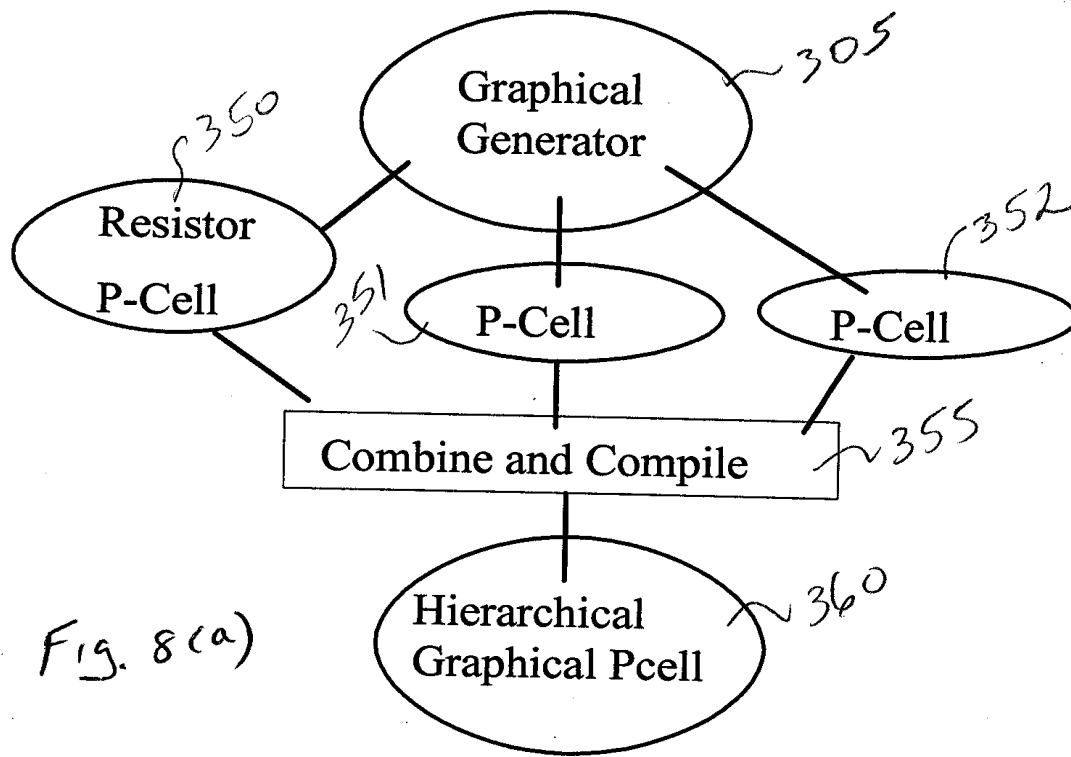
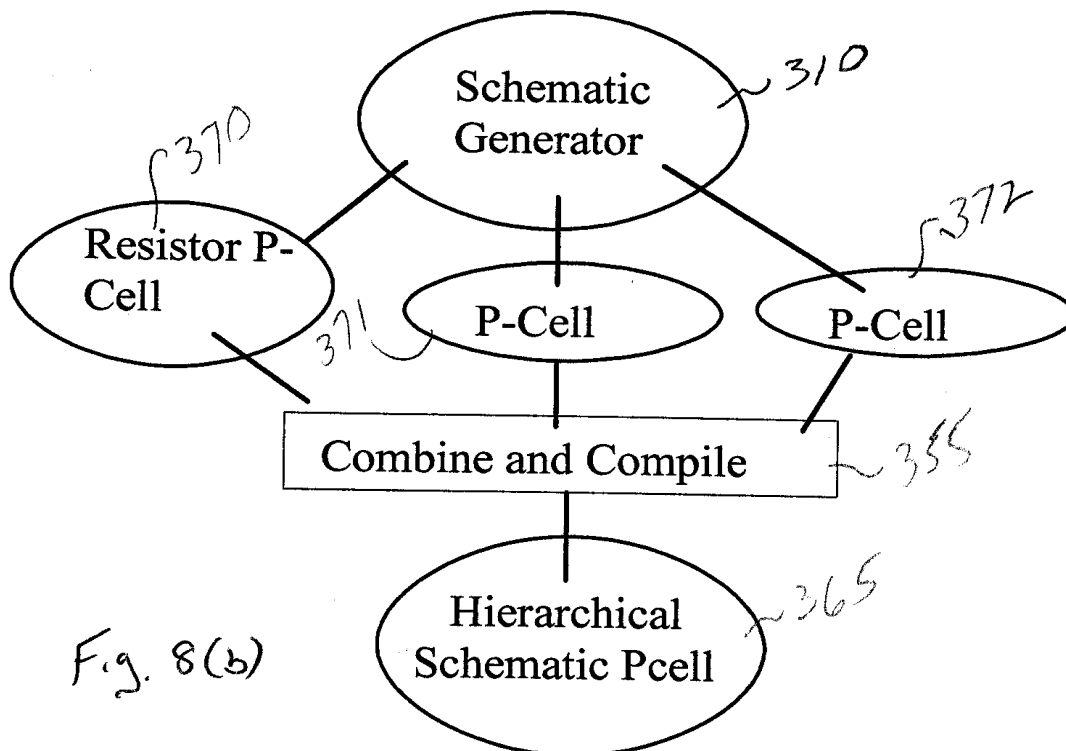


Fig. 6

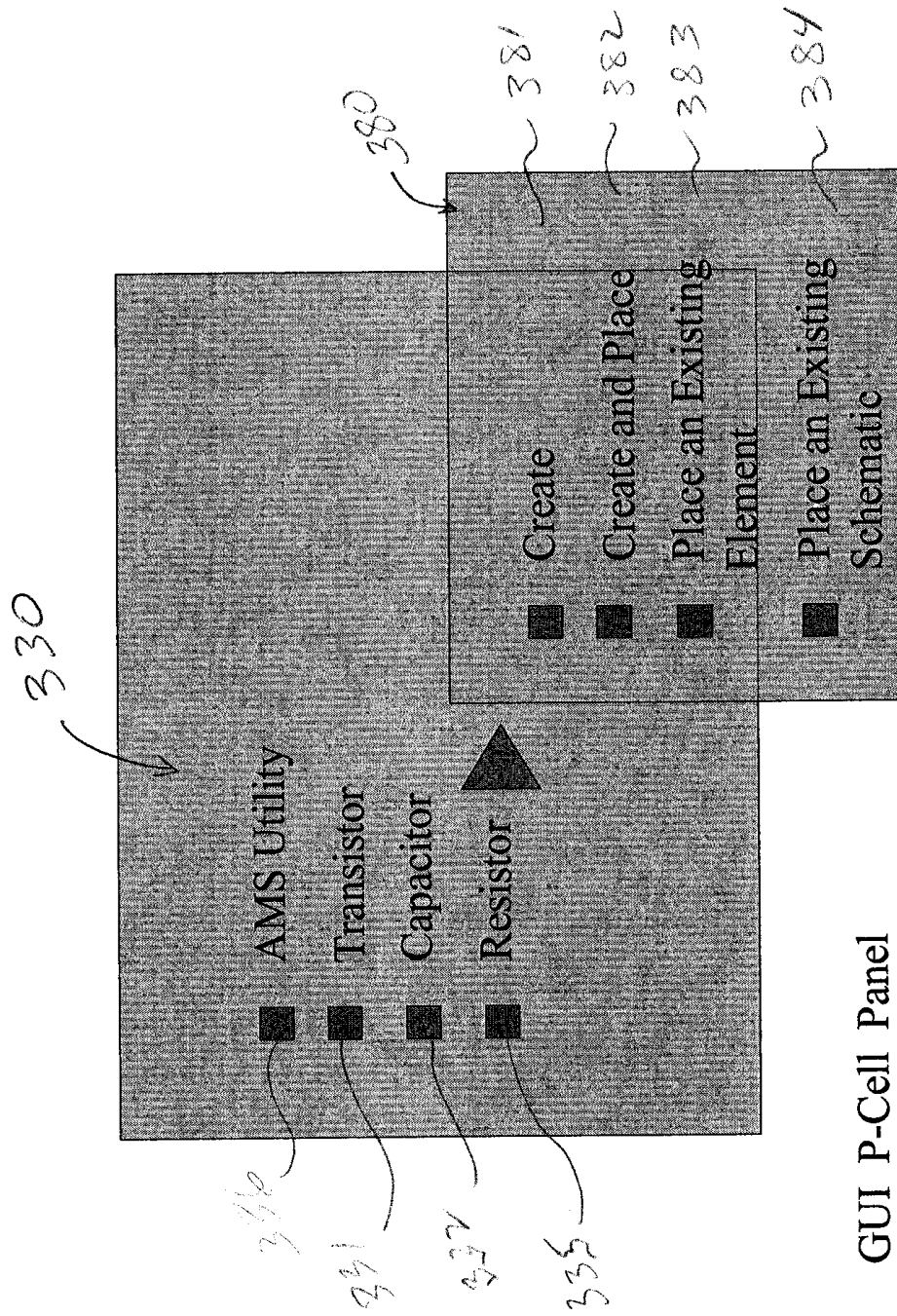
## P-Cell Graphical Design System



## P-Cell Schematic Design System







GUI P-Cell Panel

Fig. 9(a)

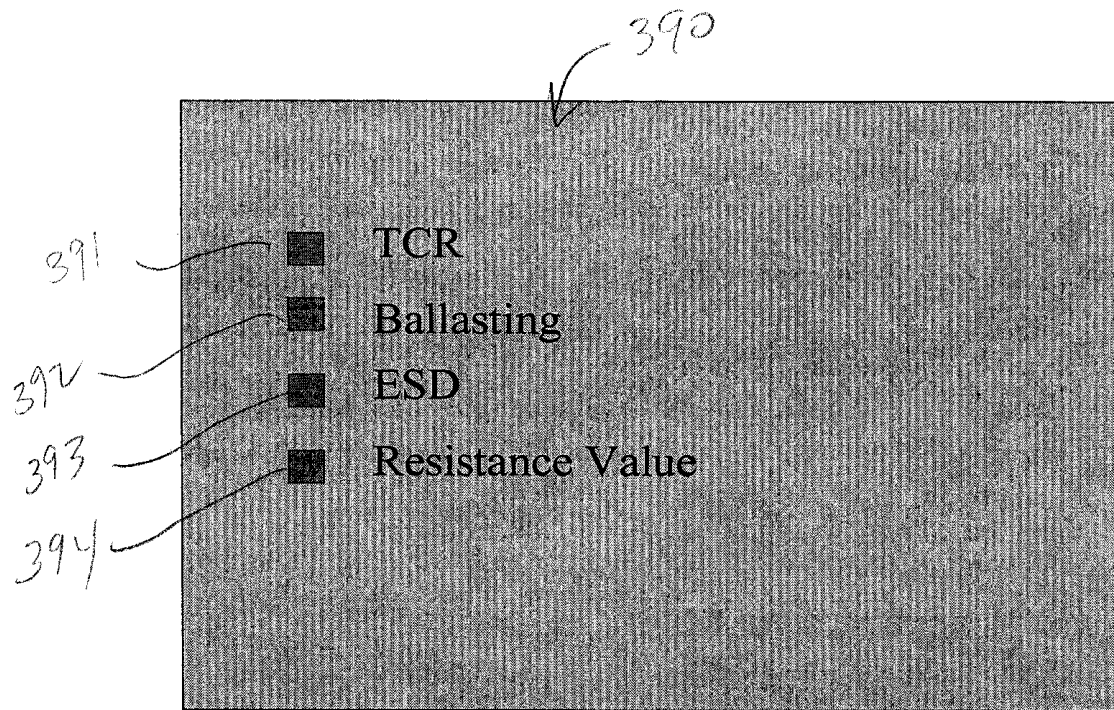


Fig. 9(b) Resistor P-Cell Panel

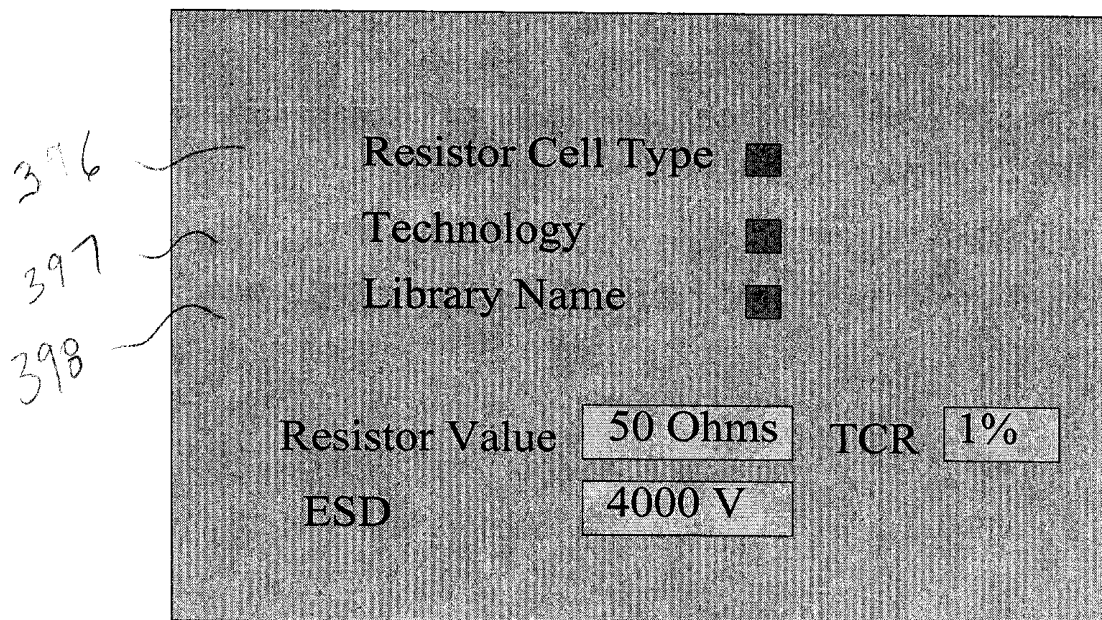


Fig. 9(c) Resistor P-Cell GUI Panel

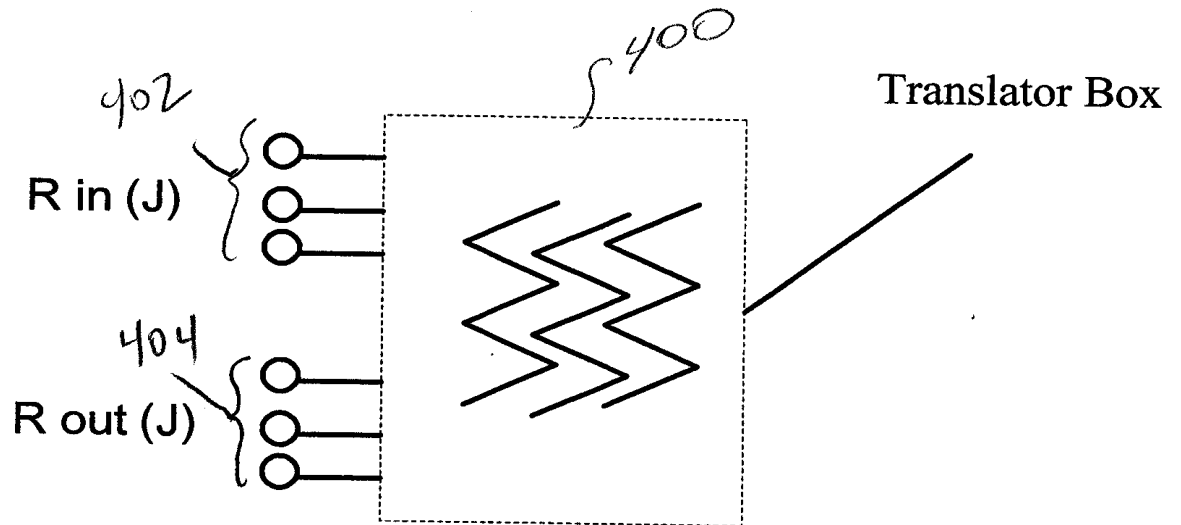


Fig. 10

Symbol Placement in Schematic Design

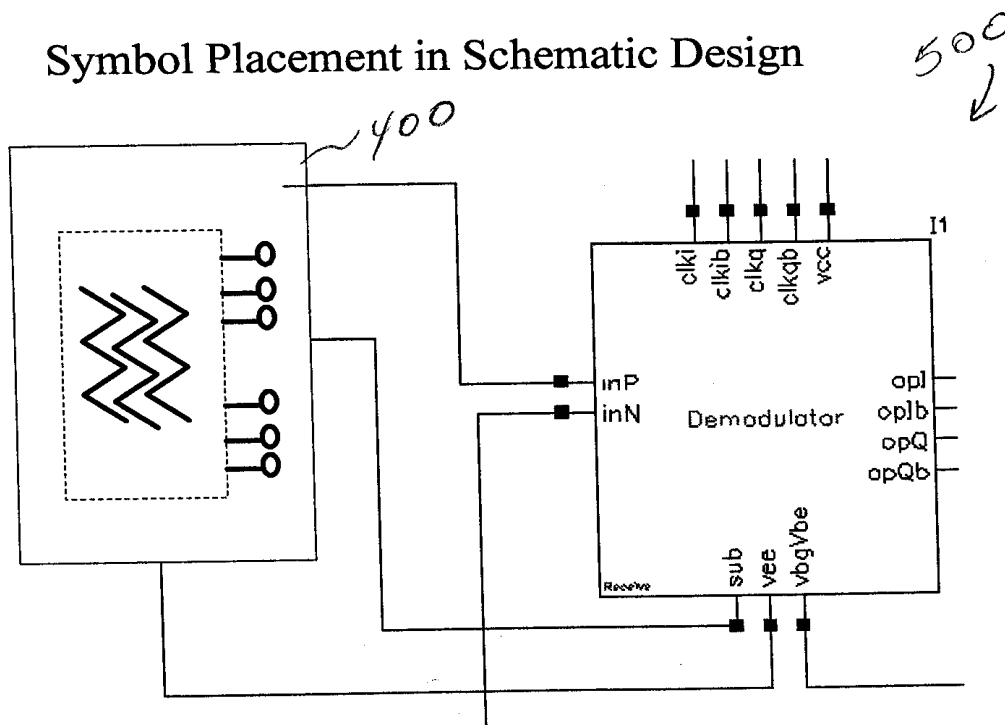


Fig. 11